

IN THE CLAIMS:

Please revise claims 1, 13, 42, 55 and 62, as indicated below.

1 1. (currently amended) Apparatus for deterring failure of a
2 computing system; said apparatus comprising:
3 an ~~exclusively~~ hardware network of components, having sub-
4 stantially no software;
5 terminals of the network for connection to such system; and
6 fabrication-preprogrammed hardware circuits of the network
7 for guarding such system from failure.

1 2. (original) apparatus of claim 1, particularly for use with
2 such system that is substantially exclusively made up of sub-
3 stantially commercial, off-the-shelf components; and wherein:
4 at least one of the network terminals is connected to re-
5 ceive at least one error signal generated by such system in event
6 of incipient failure of such system; and
7 at least one of the network terminals is connected to pro-
8 vide at least one recovery signal to such system upon receipt of
9 the error signal.

1 3. (original) The apparatus of claim 2, wherein:
2 the circuits comprise portions fabrication-preprogrammed to
3 evaluate the at least one error signal to establish characteris-
4 tics of the at least one recovery signal.

1 4. (original) The apparatus of claim 1, further comprising:
2 such computing system.

1 5. (original) The apparatus of claim 1, wherein:
2 the circuits comprise portions for identifying failure of
3 any of the circuits and correcting for the identified failure.

1 6. (original) The apparatus of claim 1, particularly for use
2 with a computing system that has at least one software subsystem
3 for conferring resistance to failure of the system; and wherein:
4 the circuits comprise substantially no portion that inter-
5 feres with such failure-resistance software subsystem.

1 7. (original) The apparatus of claim 1, particularly for use
2 with a computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that has
4 at least one hardware subsystem for generating a response of the
5 system to failure; and wherein:
6 the circuits comprise portions for reacting to said response
7 of such hardware subsystem.

1 8. (original) The apparatus of claim 1, particularly for use
2 with a computing system that has plural generally parallel
3 computing channels; and wherein:

4 the circuits comprise portions for comparing computational
5 results from such parallel channels.

1 9. (original) The apparatus of claim 8, wherein:

2 the parallel channels of the computing system are of diverse
3 design or origin.

1 10. (original) The apparatus of claim 1, particularly for use
2 with a computing system that has plural processors; and wherein:

3 the circuits comprise portions for identifying failure of
4 any of such processors and correcting for identified failure.

1 11. (original) The apparatus of claim 1, wherein:

2 the circuits comprise modules for collecting and responding
3 to data received from at least one of the terminals, said
4 modules comprising:

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6 at least three data-collecting and -responding modules,

7 and

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9 processing sections for conferring among the modules to

10 determine whether any of the modules has failed.

1 12. (original) The apparatus of claim 1, particularly for use
2 with a computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that has
4 at least one subsystem for generating a response of the system to
5 failure, and that also has at least one subsystem for receiving
6 recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis and
8 a corrective reaction between the response-generating subsystem
9 and the command-receiving subsystem.

1 13. (currently amended) Apparatus for deterring failure of
2 a computing system, wherein the computing system optionally
3 includes plural mutually redundant modules; said apparatus
4 comprising:

5 a network of components having terminals for connection to
6 such system, wherein the network is constructed to be initially
7 and permanently distinct from such computing system including all
8 of such redundant modules if present; and

9 circuits of the network for operating programs to guard such
10 system from failure;

11 the circuits comprising portions for identifying failure of
12 any of the circuits and correcting for the identified failure.

1 14. (original) The apparatus of claim 13, wherein:

2 the program-operating portions comprise a section that
3 corrects for the identified failure by taking a failed circuit
4 out of operation.

1 15. (original) The apparatus of claim 14, wherein:
2 the program-operating portions comprise a section that
3 substitutes and powers up a spare circuit for a circuit taken out
4 of operation.

1 16. (original) The apparatus of claim 13, further comprising:
2 such computing system.

1 17. (original) The apparatus of claim 13, wherein:
2 the program-operating portions comprise at least three of
3 the circuits; and
4 failure is identified at least in part by majority vote
5 among the at least three circuits.

1 18. (original) The apparatus of claim 13, particularly for use
2 with a computing system that has at least one software subsystem
3 for conferring resistance to failure of the system; and wherein:
4 the circuits comprise substantially no portion that inter-
5 feres with such failure-resistance software subsystem.

1 19. (original) The apparatus of claim 13, particularly for use
2 with a computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that has
4 at least one hardware subsystem for generating a response of the
5 system to failure; and wherein:

6 the circuits comprise portions for reacting to said response
7 of such hardware subsystem.

1 20. (original) The apparatus of claim 13, particularly for use
2 with a computing system that has plural generally parallel
3 computing channels; and wherein:

4 the circuits comprise portions for comparing computational
5 results from such parallel channels.

1 21. (original) The apparatus of claim 20, wherein:

2 the parallel channels of the computing system are of diverse
3 design or origin.

1 22. (original) The apparatus of claim 13, particularly for use
2 with a computing system that has plural processors; and wherein:

3 the circuits comprise portions for identifying failure of
4 any of such processors and correcting for identified failure.

1 23. (original) The apparatus of claim 13, wherein:
2 the circuits comprise modules for collecting and responding
3 to data received from at least one of the terminals, said modules
4 comprising:

5
6 at least three data-collecting and -responding modules,
7 and

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9 processing sections for conferring among the modules to
10 determine whether any of the modules has failed.

1 24. (original) The apparatus of claim 13, particularly for use
2 with a computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that has
4 at least one subsystem for generating a response of the system to
5 failure, and that also has at least one subsystem for receiving
6 recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis and
8 a corrective reaction between the response-generating subsystem
9 and the command-receiving subsystem.

1 25. (original) Apparatus for deterring failure of a computing
2 system that has at least one software subsystem for conferring
3 resistance to failure of the system; said apparatus comprising:
4 a network of components having terminals for connection to
5 such system; and
6 circuits of the network for operating programs to guard such
7 system from failure;
8 the circuits comprising substantially no portion that in-
9 terferes with such failure-resistance software subsystem.

1 26. (original) The apparatus of claim 25, further comprising:
2 such computing system, including such at least one software
3 subsystem.

1 27. (original) The apparatus of claim 25, particularly for use
2 with a computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that has
4 at least one hardware subsystem for generating a response of the
5 system to failure; and wherein:
6 the circuits comprise portions for reacting to said response
7 of such hardware subsystem.

1 28. (original) The apparatus of claim 25, particularly for use
2 with a computing system that has plural generally parallel
3 computing channels; and wherein:

4 the circuits comprise portions for comparing computational
5 results from such parallel channels.

1 29. (original) The apparatus of claim 28, wherein:

2 the parallel channels of the computing system are of diverse
3 design or origin.

1 30. (original) The apparatus of claim 25, particularly for use
2 with a computing system that has plural processors; and wherein:

3 the circuits comprise portions for identifying failure of
4 any of such processors and correcting for identified failure.

1 31. (original) The apparatus of claim 25, wherein:

2 the circuits comprise modules for collecting and responding
3 to data received from at least one of the terminals, said modules
4 comprising:

5
6 at least three data-collecting and -responding modules,
7 and

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9 processing sections for conferring among the modules to
10 determine whether any of the modules has failed.

1 32. (original) The apparatus of claim 25, particularly for use
2 with a computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that has
4 at least one subsystem for generating a response of the system to
5 failure, and that also has at least one subsystem for receiving
6 recovery commands; and wherein:
7 the circuits comprise portions for interposing analysis and
8 a corrective reaction between the response-generating subsystem
9 and the command-receiving subsystem.

33. (original) Apparatus for deterring failure of a
2 computing system that is substantially exclusively made of sub-
3 stantially commercial, off-the-shelf components and that has at
4 least one hardware subsystem for generating a response of the
5 system to failure; said apparatus comprising:
6 a network of components having terminals for connection to
7 such system; and
8 circuits of the network for operating programs to guard such
9 system from failure;
10 the circuits comprising portions for reacting to said re-
11 sponse of such hardware subsystem.

1 34. (original) The apparatus of claim 33, wherein:
2 the reacting portions comprise sections for evaluating the
3 hardware-subsystem response to establish characteristics of at
4 least one recovery signal.

1 35. (original) The apparatus of claim 34, wherein:
2 the reacting portions comprise sections for applying the at
3 least one recovery signal to such system.

1 36. (original) The apparatus of claim 33, further comprising:
2 such computing system, including such hardware subsystem.

1 37. (original) The apparatus of claim 33, particularly for use
2 with a computing system that has plural generally parallel
3 computing channels; and wherein:
4 the circuits comprise portions for comparing computational
5 results from such parallel channels.

1 38. (original) The apparatus of claim 37, wherein:
2 the parallel channels of the computing system are of diverse
3 design or origin.

1 39. (original) The apparatus of claim 33, particularly for use
2 with a computing system that has plural processors; and wherein:
3 the circuits comprise portions for identifying failure of
4 any of such processors and correcting for identified failure.

1 40. (original) The apparatus of claim 33, wherein:
2 the circuits comprise modules for collecting and responding
3 to data received from at least one of the terminals, said modules
4 comprising:

5
6 at least three data-collecting and -responding modules,
7 and

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9 processing sections for conferring among the modules to
10 determine whether any of the modules has failed.

1 41. (original) The apparatus of claim 33, particularly for use
2 with a computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that has
4 at least one subsystem for generating a response of the system to
5 failure, and that also has at least one subsystem for receiving
6 recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis and
8 a corrective reaction between the response-generating subsystem
9 and the command-receiving subsystem.

1 42. (currently amended) Apparatus for deterring failure of a
2 computing system that is distinct from the apparatus and that has
3 plural generally parallel computing channels; said apparatus
4 comprising:

5 a network of components having terminals for connection to
6 such system; and

7 circuits of the network for operating programs to guard such
8 system from failure, wherein such network is constructed to be
9 initially and permanently distinct from such computing system in-
10 cluding all of such parallel computing channels;

11 the circuits comprising portions for comparing computational
12 results from such parallel channels.

1 43. (previously presented) The apparatus of claim 42, wherein:
2 the parallel channels of such computing system are of di-
3 verse design or origin.

1 44. (original) The apparatus of claim 42, wherein:
2 the comparing portions comprise at least one section for
3 analyzing discrepancies between the results from such parallel
4 channels.

1 45. (original) The apparatus of claim 44, wherein:
2 the comparing portions further comprise at least one section
3 for imposing corrective action on such system in view of the
4 analyzed discrepancies.

1 46. (original) The apparatus of claim 45, wherein:
2 the at least one discrepancy-analyzing section uses a major-
3 ity voting criterion for resolving discrepancies.

1 47. (original) The apparatus of claim 42, further comprising:
2 such computing system.

1 48. (original) The apparatus of claim 47, wherein:
2 the parallel channels of the computing system are of diverse
3 design or origin.

1 49. (original) The apparatus of claim 48, wherein:
2 the comparing portions comprise circuitry for performing an
3 algorithm to validate a match that is inexact.

1 50. (original) The apparatus of ~~claim 49~~, wherein:
2 the algorithm-performing circuitry employs a degree of
3 inexactness suited to a type of computation under comparison.

1 51. (original) The apparatus of claim 49, wherein:
2 the algorithm-performing circuitry performs an algorithm
3 that selects a degree of inexactness based on type of computation
4 under comparison.

1 52. (original) The apparatus of claim 42, particularly for use
2 with a computing system that has plural processors; and wherein:
3 the circuits comprise portions for identifying failure of
4 any of such processors and correcting for identified failure.

1 53. (original) The apparatus of claim 42, wherein:
2 the circuits comprise modules for collecting and responding
3 to data received from at least one of the terminals, said modules
4 comprising:
5
6 at least three data-collecting and -responding modules,
7 and
8
9 processing sections for conferring among the modules to
10 determine whether any of the modules has failed.

1 54. (original) The apparatus of claim 42, particularly for use
2 with a computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that has
4 at least one subsystem for generating a response of the system to
5 failure, and that also has at least one subsystem for receiving
6 recovery commands; and wherein:
7 the circuits comprise portions for interposing analysis and
8 a corrective reaction between the response-generating subsystem
9 and the command-receiving subsystem.

1 55. (currently amended) Apparatus for deterring failure of a
2 computing system that has plural processors; said apparatus
3 comprising:

4 a network of components having terminals for connection to
5 such system, wherein the network is constructed to be initially
6 and permanently distinct from such computing system including all
7 of such plural processors; and

8 circuits of the network for operating programs to guard such
9 system from failure;

10 the circuits comprising portions for identifying failure of
11 any of such processors and correcting for identified failure.

1 56. (original) The apparatus of claim 55, wherein:

2 the identifying portions comprise a section that corrects
3 for the identified failure by taking a failed processor out of
4 operation.

1 57. (original) The apparatus of claim 56, wherein:

2 the section comprises parts for taking a processor out of
3 operation only in case of signals indicating that the processor
4 has failed permanently.

1 58. (original) The apparatus of claim 55, wherein:

2 the identifying portions comprise a section that substitutes
3 and powers up a spare circuit for a processor taken out of
4 operation.

1 59. (original) The apparatus of claim 55, further comprising:
2 such computing system.

1 60. (original) The apparatus of claim 55, wherein:
2 the circuits comprise modules for collecting and responding
3 to data received from at least one of the terminals, said modules
4 comprising:
5
6 at least three data-collecting and -responding modules,
7 and
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9 processing sections for conferring among the modules to
10 determine whether any of the modules has failed.

1 61. (original) The apparatus of claim 55, particularly for use
2 with a computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that has
4 at least one subsystem for generating a response of the system to
5 failure, and that also has at least one subsystem for receiving
6 recovery commands; and wherein:
7 the circuits comprise portions for interposing analysis and
8 a corrective reaction between the response-generating subsystem
9 and the command-receiving subsystem.

1 62. (currently amended) Apparatus for deterring failure of a
2 computing system; said apparatus comprising:
3 a network of components having terminals for connection to
4 such system; and
5 circuits of the network for operating programs to guard such
6 system from failure;
7 the circuits comprising modules for collecting and respond-
8 ing to data received from at least one of the terminals, said
9 modules comprising:
10
11 at least three data-collecting and -responding modules,
12 and
13
14 processing sections for conferring among the modules to
15 determine whether any of the modules has failed;
16
17 wherein the network, including all of the modules and all of
18 the processing sections, is constructed to be initially and per-
19 manently distinct from such computing system.

1 63. (original) The apparatus of claim 62, further comprising:
2 such computing system.

1 64. (original) The apparatus of claim 62, particularly for use
2 with a computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that has
4 at least one subsystem for generating a response of the system to
5 failure, and that also has at least one subsystem for receiving
6 recovery commands; and wherein:
7 the circuits comprise portions for interposing analysis and
8 a corrective reaction between the response-generating subsystem
9 and the command-receiving subsystem.

1 65. (original) Apparatus for deterring failure of a computing
2 system that is substantially exclusively made of substantially
3 commercial, off-the-shelf components and that has at least one
4 subsystem for generating a response of the system to failure, and
5 that also has at least one subsystem for receiving recovery
6 commands; said apparatus comprising:
7 a network of components having terminals for connection to
8 such system between the response-generating subsystem and the
9 ~~recovery-command-receiving subsystem; and~~
10 circuits of the network for operating programs to guard such
11 system from failure;
12 the circuits comprising portions for interposing analysis
13 and a corrective reaction between the response-generating sub-
14 system and the command-receiving subsystem.

1 66. (previously presented) The apparatus of claim 65, further
2 comprising:
3 such computing system.